PVP 14

Code: EC3T6, EE3T6

II B.Tech - I Semester–Regular/Supplementary Examinations
November 2016

SWITCHING THEORY AND LOGIC DESIGN

(Common for EEE, ECE)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Convert the gray code 1101 to binary.
b) What do you mean by self-complementing codes, give examples?
c) How can a two input X-OR gate be used as an inverter?
d) State DeMorgan's theorem.
e) What are essential prime implicants?
f) Distinguish between serial adder and parallel adder.
g) How is the size of a PLA is specified?
h) Define counter. List the types of counters.
i) What is a universal shift register?
j) List the capabilities and limitations of FSM.
k) When does two states of a sequential circuit are equivalent?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2.

a) Convert the following numbers

i. $(41.6875)_{10}$ to binary

ii. $(1001001.011)_2$ to decimal

iii. Find the 9's complement of number $(25.639)_{10}$ 8 M

b)

i. Subtract 111001 from 101011 using 2's complement

ii. What are universal gates? Realize AND, OR gates using NAND gate. 8 M

3.

a) Using Quine-McCluskey method, minimize the function

$f(W,X,Y,Z)=\sum m(0,1,5,7,8,10,14,15)$ 8 M

b) 8 M

i. Find the complement of the function F=X(Y'Z'+YZ)

ii. Reduce the following Boolean expression to two literals $F = A\bar{B}C+B+B\bar{D}+AB\bar{D}+\bar{A}C$

4.

a) Implement the full adder using decoder and OR gates.

8 M

b) Implement the following Boolean function using 4:1 MUX $F(A,B,C,D)=\sum m(0,1,2,4,6,9,12,14)$ 8 M

5.

a) Compare combinational and sequential circuits. 6 M

b) What is race around condition? How it can be eliminated ? 10 M

6. Explain the following related to sequential circuits with suitable examples.
   a) State diagram 6 M
   b) State table 5 M
   c) State assignment 5 M